IN THE CLAIMS

Please amend the claims as follows:

Claims 1-6 (Canceled).

Claim 7 (Currently Amended): A semiconductor device comprising:

a first layer;

a plurality of first test semiconductor chip elements which are arranged in the first layer;

a second layer which is different from the first layer and which has a first surface and a second surface opposed to the first surface, the first surface of the second layer being adhered to the first layer;

an opening portion which is arranged on the second surface of the second layer;

a plurality of probe pads which are arranged in the second layer and are electrically connected to the first test semiconductor chip elements through corresponding connecting members, a part of the probe pads being exposed from the opening portion; and

a plurality of second test semiconductor chip elements which are arranged in the first layer and electrically insulated from the probe pads,

wherein the second test semiconductor chip elements are of a type different from the first test semiconductor chip elements, and [[a]] the corresponding connecting ~~member~~ members ~~electrically connected to the second test elements does~~ do not exist in the second layer.

Claim 8 (Currently Amended): A semiconductor device comprising:

a first layer;

a plurality of first test semiconductor chip elements which are arranged in the first layer;

a second layer which is different from the first layer and which has a first surface and a second surface opposed to the first surface, the first surface of the second layer being adhered to the first layer;

an opening portion which is arranged on the second surface of the second layer;

a plurality of probe pads which are arranged in the second layer and are electrically connected to the first test semiconductor chip elements through corresponding connecting members, a part of the probe pads being exposed from the opening portion; and

a plurality of second test semiconductor chip elements which are arranged in the first layer and electrically insulated from the probe pads,

wherein the first test semiconductor chip elements are arranged in a first line, the second test semiconductor chip elements are arranged in a second line different from the first line, and [[a]] the corresponding connecting ~~member~~ members ~~electrically connected to the second test elements does~~ do not exist in the second layer.

Claim 9 (Currently Amended): A semiconductor device comprising:

a first layer;

a plurality of first test semiconductor chip elements which are arranged in the first layer;

a second layer which is different from the first layer and which has a first surface and a second surface opposed to the first surface, the first surface of the second layer being adhered to the first layer;

an opening portion which is arranged on the second surface of the second layer;

a plurality of probe pads which are arranged in the second layer and are electrically connected to the first test semiconductor chip elements through corresponding connecting members, a part of the probe pads being exposed from the opening portion; and

a plurality of second test semiconductor chip elements which are arranged in the first layer and electrically insulated from the probe pads,

wherein the second test semiconductor chip elements are arranged in the first layer below the probe pads, and [[a]] the corresponding connecting ~~member~~ members ~~electrically connected to the second test elements does~~ do not exist in the second layer.

Claim 10 (Canceled).

Claim 11 (Currently Amended): A semiconductor device comprising:

a first layer;

a plurality of first test semiconductor chip elements which are arranged in the first layer;

a second layer which is different from the first layer and which has a first surface and a second surface opposed to the first surface, the first surface of the second layer being adhered to the first layer;

an opening portion which is arranged on the second surface of the second layer;

a plurality of probe pads which are arranged in the second layer and are electrically connected to the first test semiconductor chip elements, a part of the probe pads being exposed from the opening portion;

a plurality of bumps which are respectively arranged on the part of the probe pads;

a third layer which is adhered to the second layer via the bumps and is different from the first and second layers;

solder balls which are arranged on the third layer and electrically connected to the first test semiconductor chip elements;

a first connection member which is arranged in the first layer and connected to the first test semiconductor chip elements;

a second connection member which is arranged in the second layer and connected to the probe pads and the first connection member;

a third connection member which is arranged in the third layer and connected to the bumps and the solder balls; and

a plurality of second test semiconductor chip elements which are arranged in the first layer and electrically insulated from the probe pads~~,~~

~~wherein a connecting member electrically connected to the second test elements does not exist in the second layer~~.

Claims 12-26 (Canceled).